REMARKS

Claims 1-20 are currently pending in the subject application and are presently under consideration. Claims 8-20 have been withdrawn from consideration.

Favorable reconsideration of the subject patent application is respectfully requested in view of the comments herein.

I. Rejection of Claims 1-7 Under 35 U.S.C. §102(e)

Claims 1-7 stand rejected under 35 U.S.C. §102(e) as being anticipated by Subramanian, *et al.* (U.S. 6,803,267) It is respectfully requested that this rejection be withdrawn for at least the following reason. Subramanian, *et al.* does not anticipate each and every limitation as recited in the subject claims.

> A single prior art reference anticipates a patent claim only if it expressly or inherently describes each and every limitation set forth in the patent claim. *Trintec Industries, Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 63 USPQ2d 1597 (Fed. Cir. 2002); *See Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the ... claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The claimed invention provides for a system and methodology for increasing the number of organic memory cells associated with a lithographic feature. In particular, *two bits of memory cells can be available for each memory cell created according to the lithographic features* of the claimed invention. Such an increase in available bits can be effected by a semiconductor structure fabrication where a selective conductive layer is sandwiched between a bit line protrusion on one side, and an electrode layer on the other side. Specifically, according to an inlay process over a substrate layer, a first electrode is formed from a bit line protrusion. Plasma enhanced CVD of a selective conductive layer, followed by an etching process, provides for the first electrode (*e.g.* bit line protrusion) to be encapsulated by the selective conductive layer. A second electrode layer can be deposited upon the first electrode and underlying substrate layer, followed by another etch process to remove the horizontal surface of the second electrode layer. Thus, the resulting structure of the memory cell exhibits *two sets of memory elements, one on each side of the first electrode* (*e.g.* bit line protrusion). Each memory element

comprises a selective conductive layer between the first and second electrode layers. Specifically, independent claim 1 recites ***...two second electrodes positioned sideways of the first electrode on walls of adjacent lithographic features of the wafer surface, to form two memory bits for one lithographic feature...***, where ***...the first electrode...*** is ***...operable with each of the second electrodes to selectively activate a memory portion of the selective conductive media...***

Subramanian, *et al.* does anticipate applicants' claimed invention. Instead, Subramanian, *et al.* relates to systems and methods for fabricating an organic memory element and/or device wherein a silicon-based resist is employed to mitigate difficulties with patterning a carbon resist deposited over an organic semiconductor. The cited reference discloses a first electrode formed in accordance with a single or dual damascene process with a dielectric layer(s), and passive material formed over the first electrode. (*See* col. 7, ln. 12-14, & ln. 39-40) Next, an organic semiconductor can be formed over the dielectric and passive material, and a silicon-based resist is formed over the organic semiconductor. (*See* col. 7, ln. 49-55, & col. 8, ln. 1-2) The resist can then be patterned, where the non-irradiated region(s) of the resist form a mask to pattern the organic semiconductor. (*See* col. 8, ln. 12, & ln. 49-50) The non-irradiated resist is stripped to expose the organic semiconductor, which forms an organic memory element within the memory structure. (*See* col.8, ln. 55-58) An upper electrode is subsequently formed on the remaining organic semiconductor material. (*See* col. 8, ln. 58-60) Thus, Subramanian, *et al.* discloses an organic memory structure that includes *an organic memory element between at least two electrodes*, wherein the organic memory element cooperates as a selectively conductive interface to operatively couple an upper electrode. (*See* col. 6, ln. 14-18) The cited reference does not disclose the novel structure of applicants' claimed invention, as Subramanian, *et al.* does not ***form two memory bits for one lithographic feature.*** While the cited reference discloses operatively coupling a second electrode to a first electrode through an organic semiconductor material (*See* Abstract), it is silent towards ***two second electrodes positioned sideways of a first electrode, where the first electrode is operable with each of the second electrodes.***

In view of at least the forgoing, it is respectfully submitted that Subramanian, *et al.* does not anticipate applicants' invention as recited in the subject claims, and withdrawal of this rejection is requested.

It is also noted that the subject matter of Subramanian, *et al.* and the claimed invention were, at the time the invention was made, subject to an obligation of assignment to Advanced Micro Devices, Inc. Accordingly, a rejection under 35 U.S.C. §103(a) would not be proper pursuant to the provisions of 35 U.S.C. §103(c).

CONCLUSION

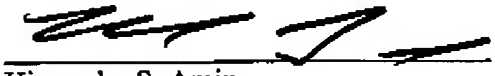
The present application is believed to be in condition for allowance in view of the above comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063[AMDP949US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

AMIN & TUROCY, LLP



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